CLAIMS

1. A junction field effect transistor (JFET) comprising:

a semiconductor substrate having a top surface and a bottom surface, wherein the top and bottom surfaces each comprise a heavily doped layer to provide an ohmic contact;

a first trench disposed in the top surface of said substrate;

a first gate region formed in the bottom of said first trench;

a first buffer region formed beneath said first gate region;

a second gate region formed beneath said first buffer region;

a second trench disposed in the top surface of said substrate adjacent to said first trench;

a third gate region formed in the bottom of said second trench;

a second buffer region formed beneath said third gate region; and

a fourth gate region formed beneath said second buffer region.

2. The JFET of Claim 1, wherein said substrate is an n-type semiconductor substrate.

3. The JFET of Claim 1, wherein said substrate is a p-type semiconductor substrate.

4. The JFET of Claim 1, wherein said first gate region has a width that is substantially equal to a width of said first buffer region.

5. The JFET of Claim 1, wherein said first gate region has a width that is less than a width of said first buffer region.

6. The JFET of Claim 1, wherein a width of said second gate region is less than a width of said first buffer region.

7. The FET of Claim 1, wherein said substrate comprises a material selected from the group consisting of silicon, gallium arsenide, silicon carbide, and gallium nitride.

8. A metal-semiconductor field effect transistor (MESFET) comprising:

a semiconductor substrate having a top surface and a bottom surface, wherein the top and bottom surfaces each comprise a heavily doped layer to provide an ohmic contact;

a first trench disposed in the top surface of said substrate;

a first gate formed on the bottom of said first trench;

a first buffer region formed beneath said first gate;

a first gate region formed beneath said first buffer region;

a second trench disposed in the top surface of said substrate adjacent to said first trench;

a second gate formed in the bottom of said second trench;

a second buffer region formed beneath said second gate region; and

a second gate region formed beneath said second buffer region.

9. The JFET of Claim 8, wherein said substrate is an n-type semiconductor substrate.

10. The JFET of Claim 8, wherein said substrate is a p-type semiconductor substrate.

11. The JFET of Claim 8, wherein said first gate has a width that is substantially equal to a width of said first buffer region.

12. The JFET of Claim 8, wherein said first gate has a width that is less than a width of said first buffer region.

13. The JFET of Claim 8, wherein a width of said first gate region is less than a width of said first buffer region.

14. The FET of Claim 8, wherein said substrate comprises a material selected from the group consisting of silicon, gallium arsenide, silicon carbide, and gallium nitride.

15. A method for fabricating a dual gate structure for a field effect transistor (FET), said method comprising:

etching a gate trench in a surface of a semiconductor substrate;

forming a first gate at the bottom of said gate trench;

implanting a buffer region beneath said first gate; and

implanting a second gate beneath said buffer region.

16. The method of Claim 15, further comprising forming a sidewall spacer to establish a width of said first gate.

17. The method of Claim 15, further comprising forming a sidewall spacer to establish a width of said buffer region.

18. The method of Claim 15, further comprising forming a sidewall spacer to establish a width of said second gate.

19. The method of Claim 15, further comprising annealing said substrate subsequent to implanting said second gate.

20. The method of Claim 15, further comprising annealing said substrate after said implanting said second gate.